

Heating rate and electrode charging measurements in a scalable, microfabricated, surface-electrode ion trap

D.T.C. Allcock¹, T.P. Harty¹, H.A. Janacek¹, N.M. Linke¹, C.J. Ballance¹, A.M. Steane¹, D.M. Lucas¹, R.L. Jarecki Jr.², S.D. Habermehl², M.G. Blain², D. Stick², D.L. Moehring²

¹ Department of Physics, University of Oxford, Clarendon Laboratory, Parks Road, Oxford, OX1 3PU, UK

² Sandia National Laboratories, Albuquerque, New Mexico 87185, USA

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Abstract We characterise the performance of a surface-electrode ion “chip” trap fabricated using established semiconductor integrated circuit and micro-electro-mechanical-system (MEMS) microfabrication processes which are in principle scalable to much larger ion trap arrays, as proposed for implementing ion trap quantum information processing. We measure rf ion micromotion parallel and perpendicular to the plane of the trap electrodes, and find that on-package capacitors reduce this to $\lesssim 10$ nm in amplitude. We also measure ion trapping lifetime, charging effects due to laser light incident on the trap electrodes, and the heating rate for a single trapped ion. The performance of this trap is found to be comparable with others of the same size scale.

1 Introduction

Many of the requirements for quantum information processing have been demonstrated using small numbers of trapped, laser-cooled ion-qubits (see [1] for a recent review). Two significant present challenges are to scale up these systems to large numbers of qubits, and to reduce the so-called “anomalous heating” affecting the ions’ external motion which is used to implement quantum logic gates between neighbouring qubits [2]. In this paper we report on the performance of a trap which is constructed using intrinsically scalable semiconductor fabrication technology. In particular we measure the motional heating rate of a single ion. The fabrication process is described in more detail in [3], where initial characterization of the trap is also reported. This trap is designed to be compatible with integration of microfabricated optical elements, and it has already been used to demonstrate collection of ion fluorescence using diffractive micro-optics [4]. Ion shuttling through junctions has also been demonstrated in traps utilising the same fabrication process [5].

2 Experimental apparatus

We tested three different traps of the same type. The traps are identical to those described in [3] except for Trap 2 which has $13\text{ }\mu\text{m}$ high oxide pillars supporting the electrodes rather than $20\text{ }\mu\text{m}$ high pillars (see fig. 1). Traps 1, 2 and 3 differ in the filtering of the dc control electrodes (see section 3). The traps were mounted in the same vacuum system used in [6]. The system was modified such that the neutral calcium oven was behind, rather than to the side of, the trap so the ions are loaded through the central slot. The oven was also loaded with isotopically enriched calcium (10% ^{43}Ca , 90% ^{40}Ca). The vacuum pressure was $< 10^{-11}$ Torr, rising to 1×10^{-11} Torr with the oven running.

The rf trapping voltage is stepped-up using an iron powder toroid (Micrometals T94-6) in a resonant transformer arrangement (see fig. 2). The toroid gives a loaded Q of 28 and a resonant frequency of $\Omega_{\text{rf}} = 2\pi \times 33\text{ MHz}$. The actual voltage step-up at the trap is 21.8, which was calculated by measuring an ion’s radial secular frequencies ω_r and deducing the trap voltage using our electric field simulation. The voltage amplitude used was in the range 50–140 V.

As the toroid does not have a high enough Q to filter out noise effectively at $\Omega_{\text{rf}} \pm \omega_r$ (which can heat the ion [7]) we place a bandpass filter between the amplifier and the toroid. The filter is a $50\text{ }\Omega$ impedance mesh-capacitor topology with 3.2 dB insertion loss at 33 MHz, -38 dBc at 30 MHz and -30 dBc at 36 MHz (typical radial frequencies are 3–4 MHz).

DC electrode voltages of up to $\pm 10\text{ V}$ are provided by an AD5372 DAC chip. This chip has an intrinsic voltage noise of $< 100\text{ nV}/\sqrt{\text{Hz}}$ but this is reduced by a further factor of $> 10^5$ by low-pass filters (RCLC topology with cut-off frequency $< 10\text{ Hz}$). The voltages after the filter board were checked for any residual noise using a spectrum analyzer and a custom pre-amplifier with a noise floor of $0.25\text{ nV}/\sqrt{\text{Hz}}$. As this trap has a similar split central control electrode configuration to an earlier trap

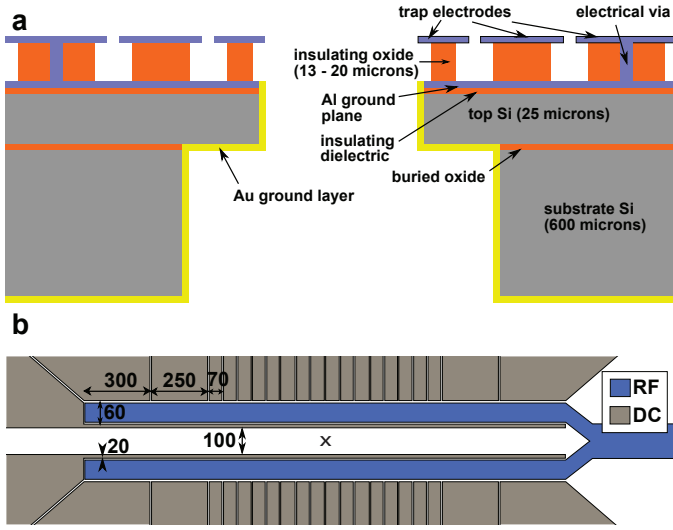


Fig. 1 Schematic diagram of the ion trap. (a) Cross-sectional view (not to scale), with layer thicknesses indicated in microns. The ion is trapped $84\mu\text{m}$ above the plane of the trap electrodes. (b) Plan view (to scale), with dimensions shown in microns. A \times marks the position of the trap centre used in these experiments.

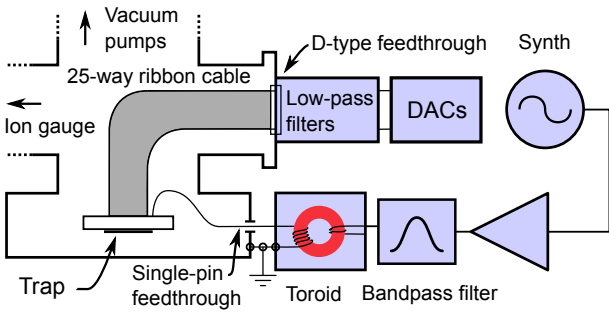


Fig. 2 Schematic of the vacuum system and wiring arrangement of the trap. The dc electrode voltages are supplied by digital-to-analogue converters (DACs), filtered by low-pass filters, and taken to the trap by a 25-way vacuum-compatible ribbon cable (we are only using the central 10 pairs of electrodes, the rest are grounded on the package). The trap rf drive is provided by a synthesizer, which is amplified and filtered, then stepped-up using a toroid in a resonant transformer arrangement. The vacuum chamber is used as the common grounding point for rf and dc voltages.

tested at Oxford, we use the same technique as in that work [6] to generate voltage sets with the required axial trapping frequency and radial principal axis orientation.

We use the same laser systems and collection optics as those described in [6]. Overall photon detection efficiency is 0.23%. This gives approximately 50,000 counts/s for a single ion cooled on the $S_{1/2}-P_{1/2}$ transition by one saturation intensity of resonant 397 nm light, and repumped on both the $D_{3/2}-P_{3/2}$ (850 nm) and $D_{5/2}-P_{3/2}$ (854 nm) transitions. Background scatter is ~ 100 counts/s at this 397 nm power ($2.0\mu\text{W}$ in a spot with $1/e^2$ radius $w = 30\mu\text{m}$) [8]. Using a multi-element diffraction-

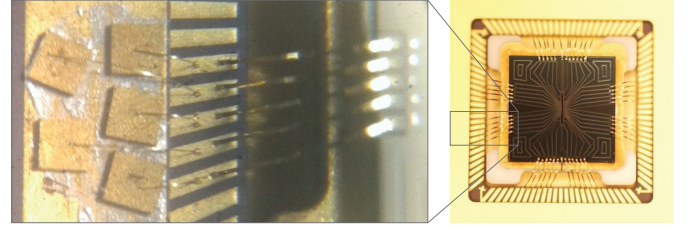


Fig. 3 Magnified view of capacitors added to the ceramic pin grid array (CPGA). The capacitors were glued to the outer, grounded, gold ring of the CPGA, and then wire bonded to the bond pads as shown.

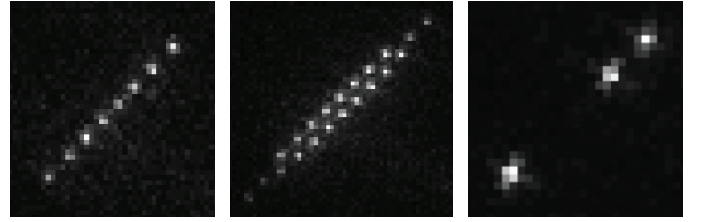


Fig. 4 8 ion $^{40}\text{Ca}^+$ crystal (left), 21 ion $^{40}\text{Ca}^+$ crystal (centre) and mixed $^{40}\text{Ca}^+$ and $^{43}\text{Ca}^+$ crystal (right). The $^{43}\text{Ca}^+$ ions are dark because the 397 nm cooling laser is not modulated to span the 3.2 GHz hyperfine splitting of the transition.

limited fibre output collimator (CVI-Melles Griot GLC-14.5-8.0-405) and quartz optics for the 397 nm beam path were important in achieving this low background.

3 Micromotion compensation

In Trap 1 we were unable to compensate the rf micromotion with static electric fields, implying that there was no stationary rf null [9]. The residual micromotion was mainly perpendicular to the plane of the trap electrodes, with an amplitude of $\sim 200\text{nm}$. This was estimated by measuring the amplitude of the micromotion sidebands on a spectrum obtained with a $D_{3/2}-P_{3/2}$ 850 nm repumping beam propagating at 45° to the plane of the trap [6]. The direction of the motion meant that we could discount a phase difference between the two rf rails, which would cause radial micromotion parallel to the plane of the trap. End effects due to the finite length of the trap were also predicted to be negligible from electric field simulations. This implied that the likely cause of the micromotion was rf pickup on the dc electrodes. For this to be the case the pickup voltages have to be out of phase with the rf electrode voltage, and the secondary rf null created by the pickup has to be in a different place to the principal rf null. We believe that in our case phase shifts were caused by the complex impedance of the $\sim 150\text{mm}$ long ribbon cable (see fig. 2) connecting the trap to the vacuum feedthrough or by crosstalk between the wires in the cable.

In an effort to reduce the micromotion in Trap 1 we added a low voltage “compensation” rf voltage to

one of the central dc electrodes. This rf was supplied by a synthesizer phase-locked with a variable offset to the main rf drive synth. By adjusting the phase offset and the amplitude of this synthesizer we were able to eliminate the micromotion parallel to the trap surface. This implied that a significant cause of the problem was rf pickup on these centre electrodes, which might be expected since, out of all the dc electrodes, they have by far the largest capacitive coupling to the rf electrodes and therefore will have the largest rf pickup. On Trap 2, therefore, we added a 1 nF capacitor to the package between each of these electrodes and the trap ground plane. However, significant micromotion perpendicular to the trap surface was still present, so on trap 3 we added a 820 pF capacitor between each dc electrode and ground. These capacitors were glued onto the outer gold ring of the CPGA with Epo-Tek H20E conductive epoxy and then wire bonded to the pads on the CPGA (see fig. 3). These capacitors have the effect of moving the common rf grounding point onto the trap package, eliminating differential phase-shifts due to the ribbon cable.

The addition of these capacitors reduced the residual micromotion to a similar amplitude to that caused by a 1 V/m (10 V/m) excess field parallel (perpendicular) to the plane of the trap (at 2.35 MHz radial secular frequency). This implied there was a residual motion of order 1 nm (10 nm), which is at the limit of what we can conveniently resolve with our compensation technique [6].

4 Trapping lifetime

Single-ion trapping lifetime was of order one hour with laser cooling and of order one minute without. In traps 1 and 2 the two-ion lifetime was only a few minutes (with cooling) and we were unable to load large crystals. In trap 3 the two-ion lifetime was approximately half the single-ion lifetime and we were able to load large crystals with tens of ions (see fig. 4). The difference in behaviour is likely to be because, with multiple ions, micromotion causes parametric heating when the ions are hot and the motion becomes anharmonic [7] (for example, after a background gas collision or just after loading). We have also successfully loaded $^{43}\text{Ca}^+$ ions and sympathetically cooled them using $^{40}\text{Ca}^+$ ions [10].

5 Charging effects

The traps appear to be fairly resistant to charging under normal operation. The field compensation in the direction parallel to the trap plane drifts by only ~ 1 V/m on an hour timescale with no change during or after ion re-loading.

A more detailed study of the trap charging was conducted by irradiating the electrodes directly with a 397 nm laser beam to induce a larger charging effect. The beam

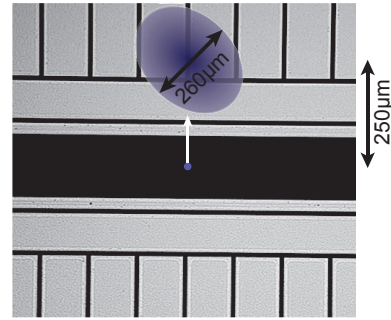


Fig. 5 Diagram to show how the 397 nm charging beam strikes the trap. The beam has a circular profile with spot size $w = 130 \mu\text{m}$, but propagates at 45° to the surface so it illuminates an elliptical area of the electrodes. The white arrow shows the direction of the induced electric field measured at the ion (blue dot).

had a power of $10 \mu\text{W}$ in a circular spot with $1/e^2$ radius $w = 130 \mu\text{m}$ and propagated at 45° to the surface (see fig. 5). Data were taken by turning the laser on for a fixed amount of time, then repeatedly recompensating the in-plane micromotion at ~ 30 s intervals. This method has a resolution of ± 1 V/m with 10 s detection time. Both the direction of the resulting field (which attracted the ion towards the beam spot) and the time dependence of its decay were in agreement with previous work by Harlander and coworkers [11]. The data are well fitted by a double exponential (see fig. 6) with time constants 77.5 and 654 seconds compared to 5 and 120 seconds reported in that work. This is possibly because the native oxide layer on our aluminium trap was thicker or less conductive than that on the copper trap in [11] and could support a longer relaxation time for any charges on it [12].

6 Heating rates

We made several studies of the heating rate in Trap 3 using our simplified method for Λ systems [6] based on that described in [13]. We see no significant effect on the heating rate due to variations in the radial frequency (fig. 7a) which implies that we are observing axial mode heating only. The heating rate dependence on the axial frequency (see fig. 7b) below $f \approx 750$ kHz is comparable with the $1/f$ dependence reported in the literature [2, 14, 15]. Above 750 kHz the frequency dependence is weaker which means either that the noise in our system does not have a simple $1/f^n$ dependence or that there is another noise source with a different frequency dependence that dominates at higher frequencies. The data in fig. 7 were taken at the centre of the trap but we measured the same heating rates at locations $\pm 270 \mu\text{m}$ along the trap z -axis.

We also attempted to measure the heating rate in Trap 2 but it exhibited a strong dependence on the rf

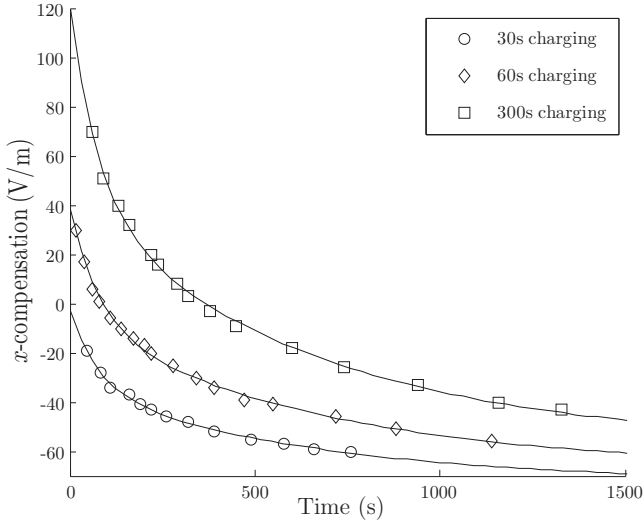


Fig. 6 Electric field measured at the ion, after irradiation of the trap by 30, 60 and 300 s exposure to the 397 nm charging beam. The curves are a joint fit to $E_x = A_i + B_i e^{-t/t_1} + C_i e^{-t/t_2}$ and the fitted time constants are $t_1 = 78$ s and $t_2 = 654$ s. Errors are approximately the size of the symbols used.

drive amplitude pointing to a heating contribution from the radial modes. This, together with the large micromotion amplitude, renders a simple one-dimensional heating rate model inapplicable. We did note a large increase in heating rate without the rf filter in Trap 2; this is to be expected since an uncompensated trap is very sensitive to noise at $\Omega_{\text{rf}} \pm \omega_r$ [16]. In trap 3, however, we measured no heating rate increase with variations in the out-of-plane compensation field (up to ~ 100 V/m) or when running the trap without the rf filter.

7 Future Improvements

7.1 Coated electrodes

Comparisons made by Wang and coworkers [17] indicate that coating the trap with another material, such as gold, which does not support a native oxide layer will reduce the charging measured in section 5 by more than an order of magnitude. For this design of trap, evaporative coating is straightforward as the electrodes themselves act as a shadow mask to prevent shorting. As this evaporation can be done as a final processing step after packaging, even materials like gold (see fig. 8) which are not compatible with CMOS fabrication can be used. A similar gold coated trap has been tested and ions have been loaded into it and shuttled without problems, though detailed studies are yet to be carried out.

7.2 Integrated filters

As demonstrated in section 3, it is necessary to minimize rf pickup on control electrodes, and hence placement of

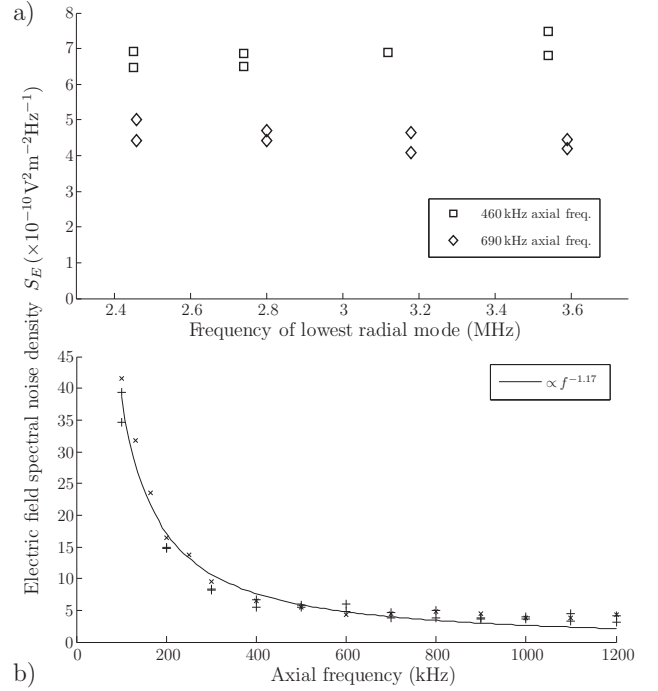


Fig. 7 Single-ion heating rate in Trap 3, expressed as the electric field spectral noise density experienced by the ion. (a) Heating rate versus radial frequency at fixed axial frequencies of $f_z = 460$ kHz and $f_z = 690$ kHz. (b) Heating rate versus axial frequency at fixed rf amplitude ($f_{r1} \simeq 3.1$ MHz, $f_{r2} \simeq 3.5$ MHz). The data points marked (x) were taken a week after those marked (+). The curve is the least-squares fit to a $1/f^n$ power law. The heating rate equates to ~ 55 quanta/ms at 1 MHz axial frequency.

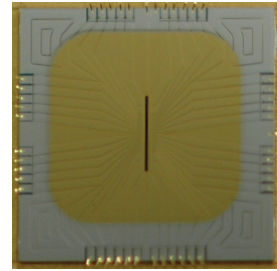


Fig. 8 A trap where the ion trapping region has been evaporatively coated with gold.

capacitive filters in the closest possible proximity to the electrodes is optimal. Additionally, filtering with a cut-off frequency larger than the DAC update rate and smaller than the rf drive and ion secular frequencies is required. For a 1 MHz cut-off frequency, a capacitor value of 1 nF and a resistor value of 1 k Ω can be integrated directly into the trap chip itself as part of the chip fabrication process.

While it is possible to monolithically integrate planar (horizontal) metal-insulator-metal plate capacitors on surface electrode traps, we find that a reliable, defect-free capacitor insulating layer using plasma deposited

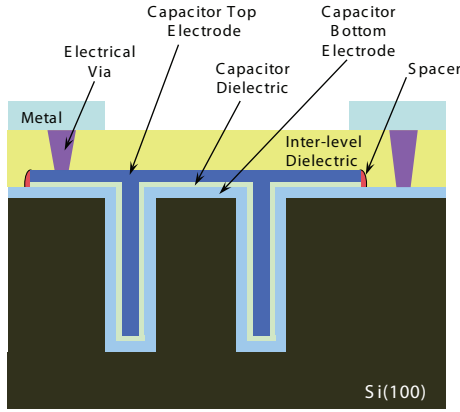


Fig. 9 Schematic of trench capacitors built into the ion trap chip Si substrate.

silicon nitride requires 30 to 50 nanometers in dielectric thickness, resulting in areal capacitance values of approximately $dC/dA = 1.3$ to $2.1 \text{ fF}/\mu\text{m}^2$ and capacitor plate areas approaching 1 mm^2 per electrode. The trap chip real estate requirement quickly becomes prohibitively large for more than a few tens of electrodes. Alternatives for increasing the areal capacitance values (thus decreasing the capacitor area) include using a high- k dielectric and thinning the dielectric. The former provides quite modest improvements while the latter presents yield and reliability challenges, particularly with plasma deposited dielectrics.

A much more attractive alternative is to use low pressure chemical vapor deposited (LPCVD) dielectric films (for example stoichiometric Si_3N_4) to achieve a reliable insulator at thicknesses of 5 to 20 nm and to create more available capacitor area by using vertical surfaces (see for example [18]). Fig. 9 shows schematically the configuration of such “trench” capacitors. By building capacitors in vertical trenches etched in the Si surface of the trap chip, capacitance values on the order of 1 nF may be achieved in horizontal (chip surface) areas of order $100 \times 100 \mu\text{m}^2$. As an example of this, Fig. 10 below shows capacitance as a function of the chip surface area used for both trench and plate (horizontal, surface) capacitors for a 20 nm Si_3N_4 dielectric. Vertical trenches of width $0.5 \mu\text{m}$ and pitch $1.0 \mu\text{m}$ were etched $13 \mu\text{m}$ deep in the Si substrate and phosphorus-doped LPCVD Si served as the top and bottom capacitor plates. A factor of 30 improvement is demonstrated for the trench capacitors. These vertical trench capacitors may be integrated with the surface electrode traps described in this work.

8 Conclusion

We have further characterized the performance of the microfabricated surface-electrode trap described in [3], quantifying the heating rate of a single trapped ion, the charging effects on the trap by 397 nm laser light, the

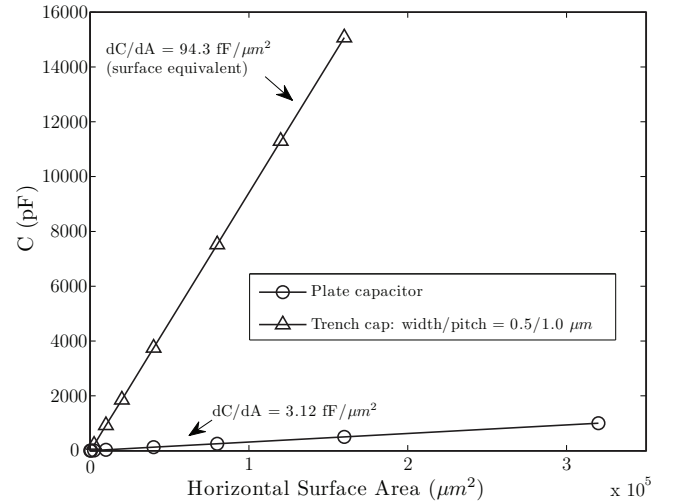


Fig. 10 Capacitance values as a function of horizontal chip surface area consumed for vertical trench (Δ) and surface plate (\circ) capacitors. The capacitor dielectric was 20 nm LPCVD Si_3N_4 .

ion micromotion parallel and perpendicular to the trap surface, and the ion lifetime. It was found to be essential to place capacitive filters close to the dc electrodes to prevent rf pickup and allow compensation of the ion micromotion. We described how in a future version of the design “trench” capacitors could be integrated on-chip to fulfil this function. We were able to load ion crystals and demonstrate sympathetic cooling of $^{43}\text{Ca}^+$ ions by $^{40}\text{Ca}^+$.

The heating rate observed in this trap is comparable to that measured in other traps of similar ion-electrode distance scale [19]; however, this trap has the important advantage that it is readily scalable to larger electrode arrays through the demonstrated use of junctions [5], as envisaged for an ion trap quantum information processor [20, 21]. Furthermore, since the underlying trap device integration technique is based largely on established semiconductor integrated circuit and MEMS (micro-electro-mechanical-system) microfabrication processes, it is readily amenable to the additional integration of CMOS logic, DAC controllers and micro-optics for qubit manipulation and detection.

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References

1. D Wineland and D Leibfried. Quantum information processing and metrology with trapped ions. *Laser Physics Letters*, 2011.
2. Q A Turchette, D Kielpinski, B E King, D Leibfried, D M Meekhof, C J Myatt, M A Rowe, C A Sackett, C S Wood, W M Itano, C Monroe, and D J Wineland. Heating of trapped ions from the quantum ground state. *Physical Review A*, 2000.
3. D Stick, K M Fortier, R Haltli, C Highstrete, D L Moehring, C Tigges, and M G Blain. Demonstration of a microfabricated surface electrode ion trap. *arXiv, physics.ins-det*, 2010.
4. G Brady, A Ellis, D Moehring, D Stick, C Highstrete, K M Fortier, M G Blain, R A Haltli, A A Cruz-Cabrera, R D Briggs, J R Wendt, T R Carter, S Samora, and S A Kemme. Integration of fluorescence collection optics with a microfabricated surface electrode ion trap. *Applied Physics B: Lasers and Optics*, 2010.
5. D L Moehring, C Highstrete, D Stick, K M Fortier, R Haltli, C Tigges, and M G Blain. Design, fabrication, and experimental demonstration of junction surface ion traps. *arXiv, quant-ph*, 2011. 9 pages, 6 figures.
6. D T C Allcock, J A Sherman, D N Stacey, A H Burrell, M J Curtis, G Imreh, N M Linke, D J Szwer, S C Webster, A M Steane, and D M Lucas. Implementation of a symmetric surface-electrode ion trap with field compensation using a modulated Raman effect. *New Journal of Physics*, 2010.
7. D Wineland, C Monroe, W M Itano, D Leibfried, B E King, and D M Meekhof. Experimental issues in coherent quantum-state manipulation of trapped atomic ions. *Journal of Research of the National Institute of Standards and Technology*, 1998.
8. N Linke et al. Doppler cooling with zero background using dipole transitions only. To be published, 2011.
9. D Berkeland, J Miller, J C Bergquist, W M Itano, and D J Wineland. Minimization of ion micromotion in a paul trap. *Journal of Applied Physics*, 1998.
10. B Blinov, L Deslauriers, P Lee, M Madsen, R Miller, and C Monroe. Sympathetic cooling of trapped Cd^+ isotopes. *Physical Review A*, 2002.
11. M Harlander, M Brownnutt, W Hänsel, and R Blatt. Trapped-ion probing of light-induced charging effects on dielectrics. *New Journal of Physics*, 2010.
12. M Rageh, D V Morgan, and A E Guile. Charge storage and the effect of ultraviolet radiation on aluminium oxide films. *Journal of Physics D: Applied Physics*, 1977.
13. J Wesenberg, R Epstein, D Leibfried, R B Blakestad, J Britton, J P Home, W M Itano, J D Jost, E Knill, C Langer, S Seidelin, and D J Wineland. Fluorescence during doppler cooling of a single trapped atom. *Physical Review A*, 2007.
14. L Deslauriers, S Olmschenk, D Stick, W K Hensinger, J Sterk, and C Monroe. Scaling and suppression of anomalous heating in ion traps. *Physical Review Letters*, 2006.
15. J Labaziewicz, Y Ge, P Antohi, D Leibbrandt, K R Brown, and I L Chuang. Suppression of heating rates in cryogenic surface-electrode ion traps. *Physical Review Letters*, 2008.
16. R Blakestad. Transport of trapped-ion qubits within a scalable quantum processor. *Thesis*, 2010.
17. SX Wang, N Lachenmyer, Y Ge, G Low, P Herskind, and I L Chuang. Laser-induced charging of microfabricated ion traps. Poster presented at Workshop on Ion Trap Technology 2011, Boulder CO.
18. J vom Dorp, T Erlbacher, A J Bauer, H Ryssel, and L Frey. Dielectric layers suitable for high voltage integrated trench capacitors. *Journal of Vacuum Science and Technology B*, 2011.
19. J M Amini, J Britton, D Leibfried, and D J Wineland. Microfabricated chip traps for ions. *arXiv, quant-ph*, 2008.
20. D Kielpinsky, C Monroe, and D J Wineland. Architecture for a large-scale ion-trap quantum computer. *Nature*, 2002.
21. A M Steane. How to build a 300 bit, 1 giga-operation quantum computer. *Quantum Information and Computation*, 2007.